Leakage Variation with Aspect Ratio in ALD High-K ZrO_2 Dielectrics

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ALD 2020

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EMD ELECTRONICS

high-throughput experimentation and expertise for faster memory innovation at intermolecular

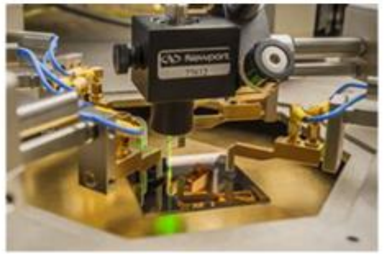
World's largest high-throughput thin-film facility

Facility highlights
(1) 45,000 sf lab space
(2) 11 cluster tool platforms
(3) 19 PVD chambers
(4) 15 ALD chamber
(5) 85 people
(6) ~1/2 with advanced degree

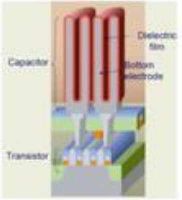
Combinatorial Wafer with ALD quadrants and PVD spots

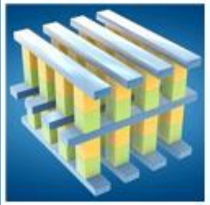
Example Cluster Tool Platform

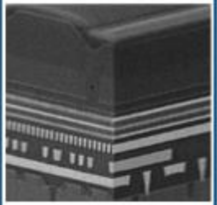
Advanced film characterization (XRF, XRR, XRD, XPS, VASE, etc.) and world-class etest capabilities



10+ years experience in memory

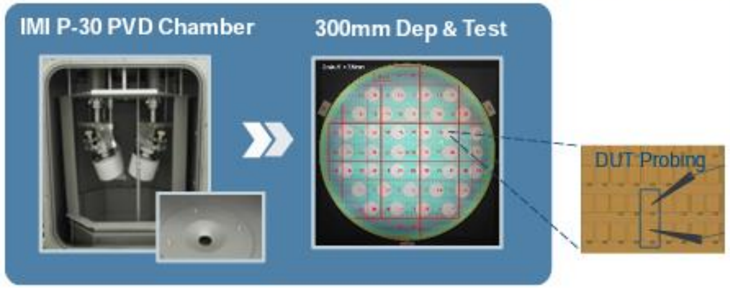


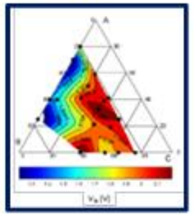




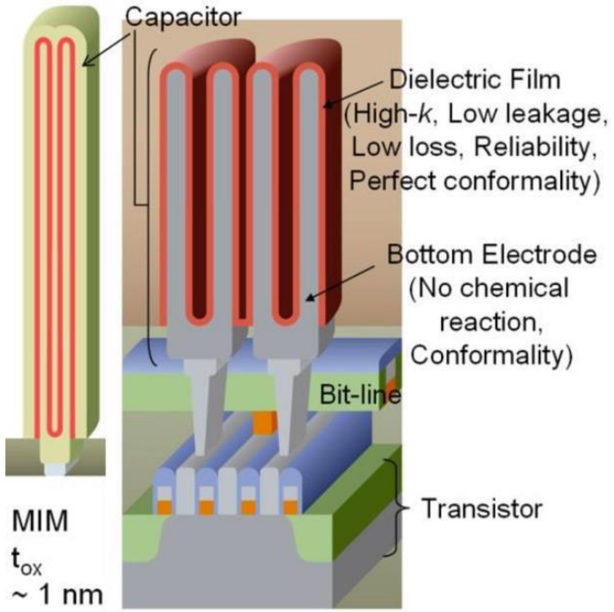
	DRAM	PCRAM	ReRAM
Focus	Capacitor	OTS Selector	ReRAM cell
Materials	High-K & High WF	Chalcogenides	Switching, Enabler, Contacts
Processes	ALD, PVD, anneal	ALD, PVD, anneal	ALD, PVD, anneal
Device	MIMCAP, customer	MIMCAP, customer	MIMCAP, customer
Main Metrics	Cap: J - EOT	OTS: J, V_{th}, V_{hold}	R_{On}/R_{Off}, V_{sw}, I_{sw}

Successfully screened 1000's of OTS, MSM, MIEC and TMO selector compositions





Denser Memory Enabled by ALD



Challenge: Scaling DRAM capacitors

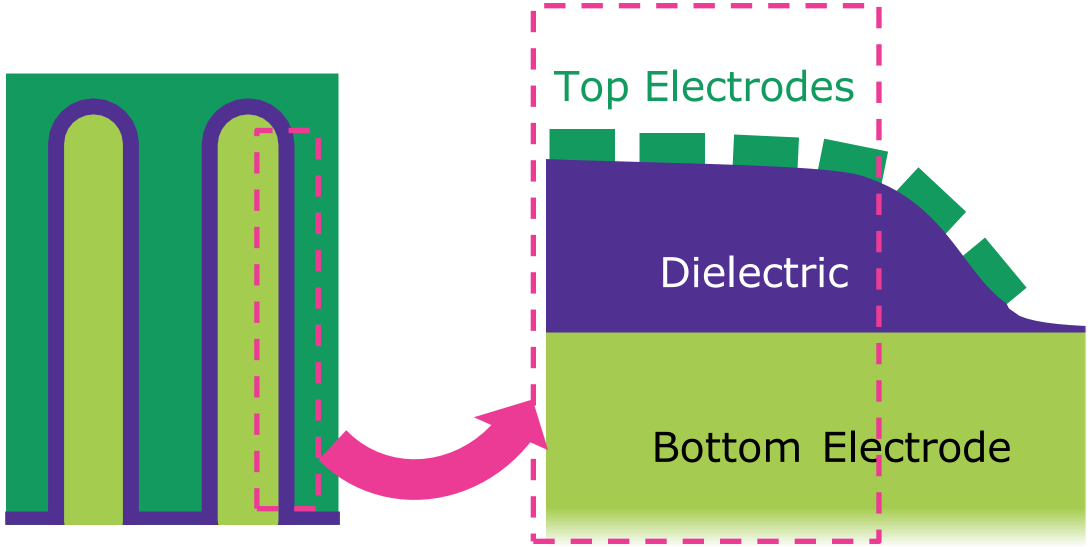
- Denser packing of memory elements ➔ higher storage density, lower voltage operation
- Large capacitor areas by "folded up" 3D geometry
  - Ultrathin dielectric sandwiched between electrodes

$$C = \kappa \varepsilon_0 \frac{A}{d}$$

Conformal ALD high-*K* dielectrics with low leakage

- High aspect ratio (HAR) ALD
- Conformality limits device density
- *Changes in material properties with trench depth?*

Our approach to investigating HAR-ALD:



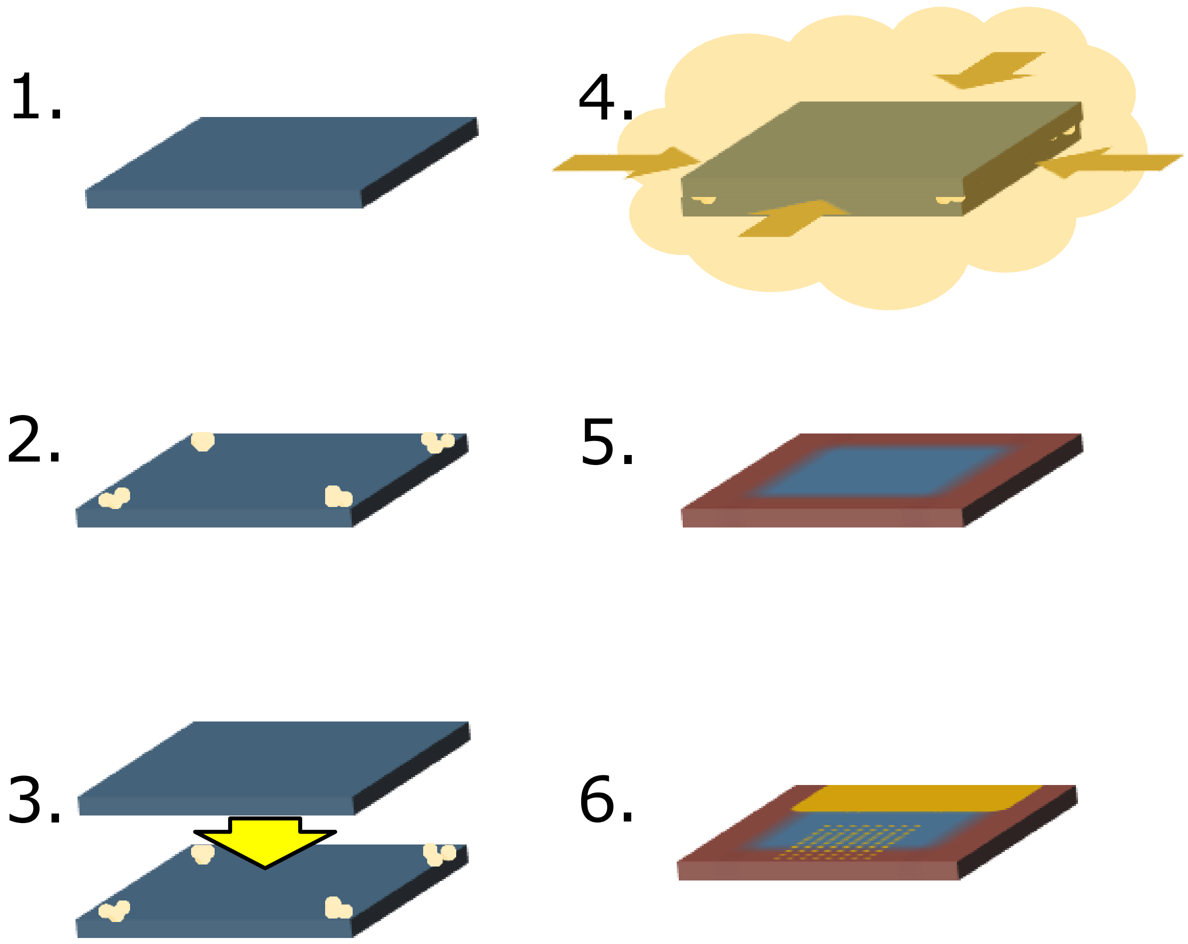
Clark *et al.*, *Materials* **7** (2014) 2913

HAR Test Vehicle by Intermolecular

U.S. patent application 16/714,934

Projects nanoscale HAR phenomena onto the >100 µm scale for study by standard metrology.

1. Start with a flat coupon (typically 44mm).
2. Apply monodisperse micro-beads to corners.
3. Place a flat cover coupon.
4. Load into reactor and perform ALD.
5. Remove cover and beads. Perform metrology along film gradient.
6. Perform post-processing and deposit any additional layers. Add top contacts for electrical testing.



Trench geometry can be related to circular vias using the **equivalent aspect ratio** (EAR):*

$$AR_{trench} = L/w$$

$$EAR_{via} = L/(2w)$$

L : Distance from edge of coupon

w : Spacing between coupons

*Cremers *et al.*, *Appl. Phys. Rev.* **6** (2019) 021302

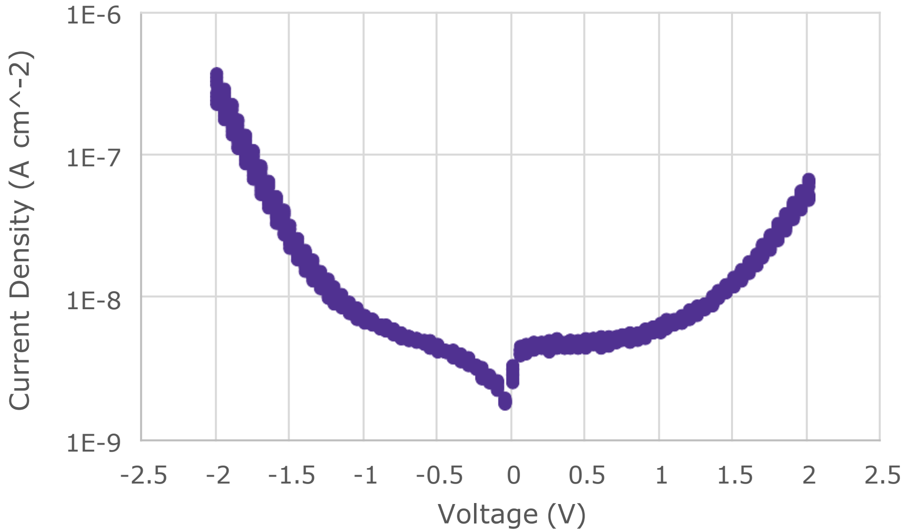
Test vehicle useful for EAR_{via} up to ~400

MIMcap Model Capacitor

- Blanket PVD TiN (bottom electrode)
- ALD ZrO_2 (dielectric)
  - *80 cycles amide-type Zr precursor / 4% O_3*
    - *250 °C, 1 Torr*
- Shadow masked PVD TiN (top electrodes)
  - *254 µm dia.*
- Post-metal anneal (450 °C in N_2, 5 min.)

Good capacitor performance

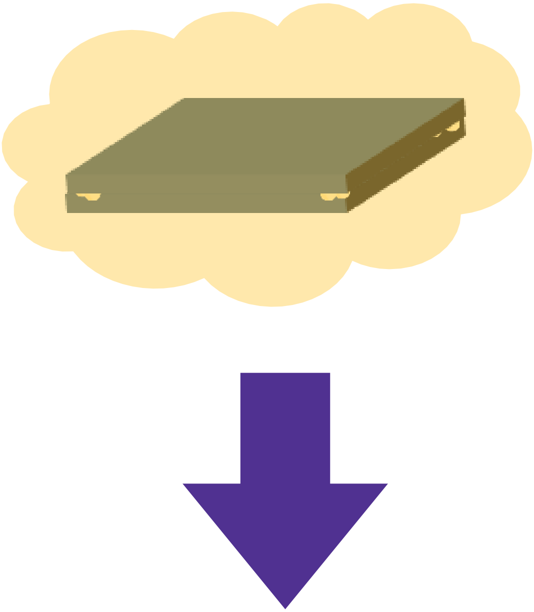
- Low leakage current
- k = 24.5(4) (0 V capacitance measurement)

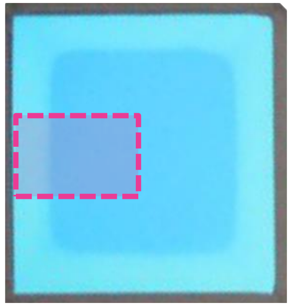


MIMcap Model DRAM Capacitors by HAR-ALD

- Blanket PVD TiN (bottom electrode)
- HAR-ALD ZrO_2 (dielectric)
  - *80 cycles amide-type Zr precursor / 4% O_3*
    - *250 °C, 1 Torr*
  - *SiO_2 microbead spacer diameter: $w = 50\ \mu m$*
  - *Reactant Knudsen number: $\lambda/w \approx 0.7$*
    - *Transitional flow (not molecular flow)*

- Shadow masked PVD TiN (top electrodes)
  - *203 µm dia.*
- Post-metal anneal (450 °C in N_2, 5 min.)



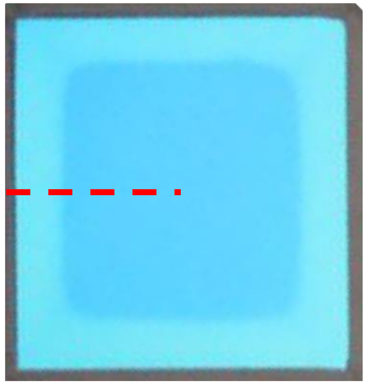


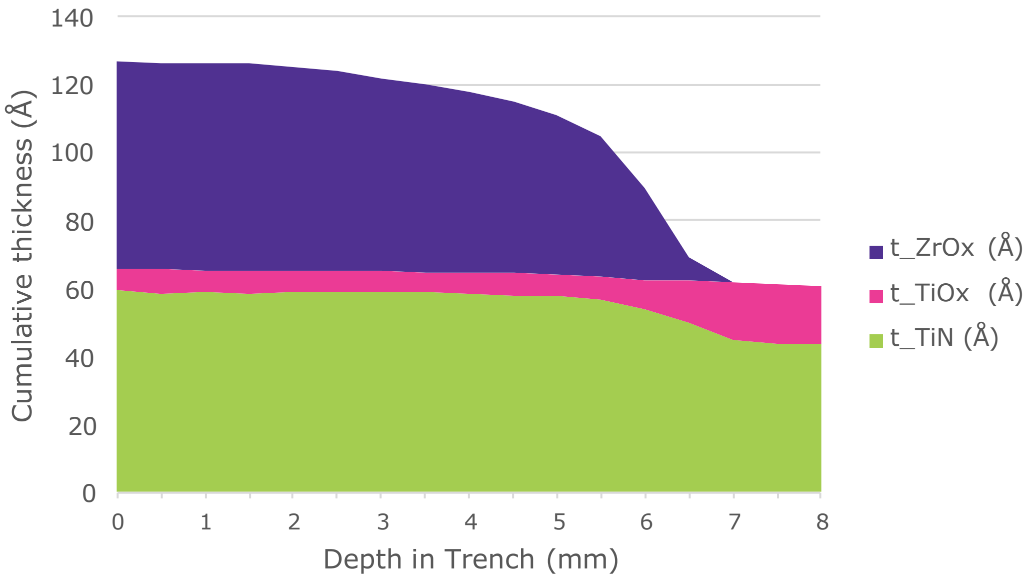
MIMcap Model DRAM Capacitors by HAR-ALD

Film thickness profile measured by ellipsometry

- Poor fit when assuming a SiO_x/TiN/ZrO_x stack
- Better fits when assuming the TiN electrode surface oxidizes to TiO_x
  - Few-Å TiO_x layer below ZrO_2
  - Thickens toward end of the ZrO_2 film as ozone migrates deeper into the HAR trench

Representative HAR-ALD sample appearance and ellipsometer line scan location:

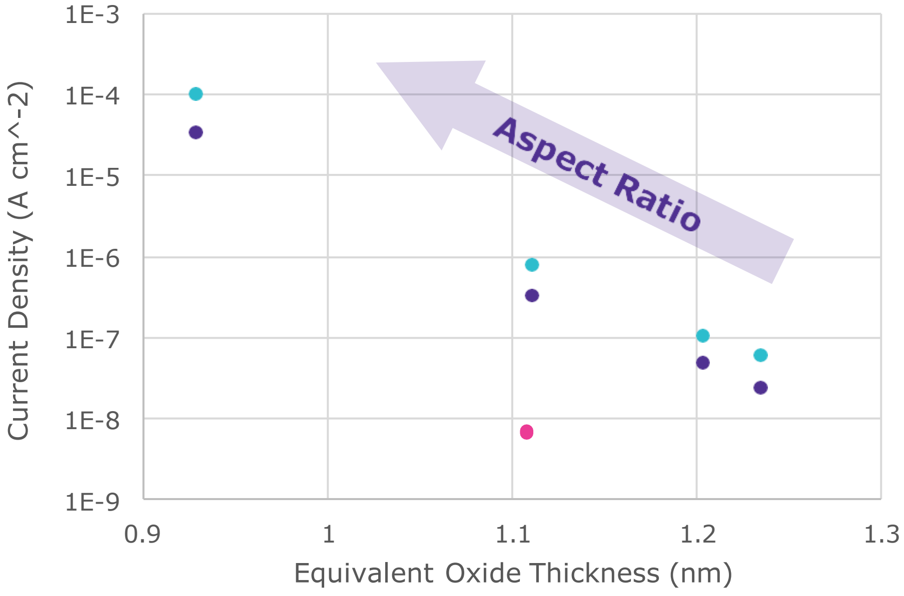


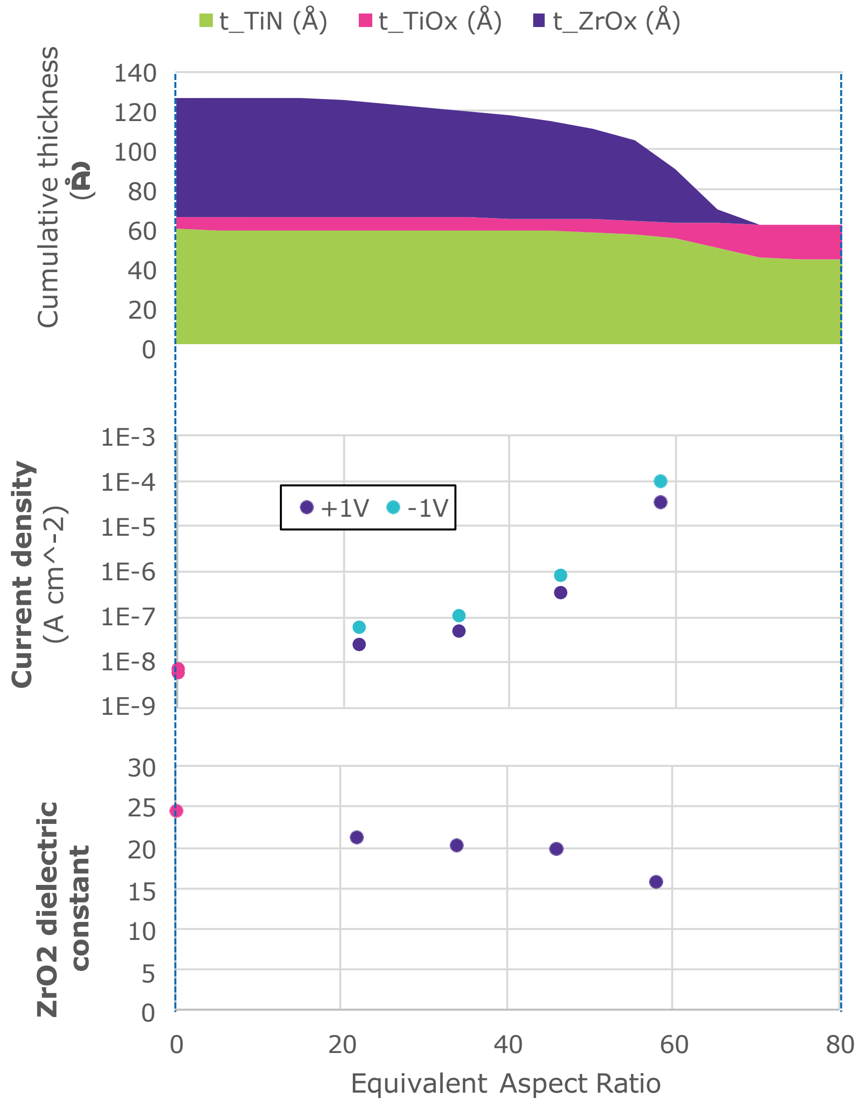


MIMcap Performance vs. Aspect Ratio

- Electrical testing shows changes in electrical properties with equivalent aspect ratio:
  - Higher leakage with depth, as expected for a thinning film
  - Lower ZrO_2 dielectric constant with depth

➔ Significantly worse performance of HAR-ALD ZrO_2 vs. blanket ALD ZrO_2





HAR-ALD Platform for Mechanism Understanding

Remaining Questions:

What causes higher leakage for HAR-ALD ZrO_2 vs. blanket ZrO_2?

➔ How does reaction chemistry change with depth into the trench?

➔ Macroscale HAR-ALD platform enables metrology (XPS, XRD, synchrotron techniques)

➔ How can the process be modified for more consistent performance?

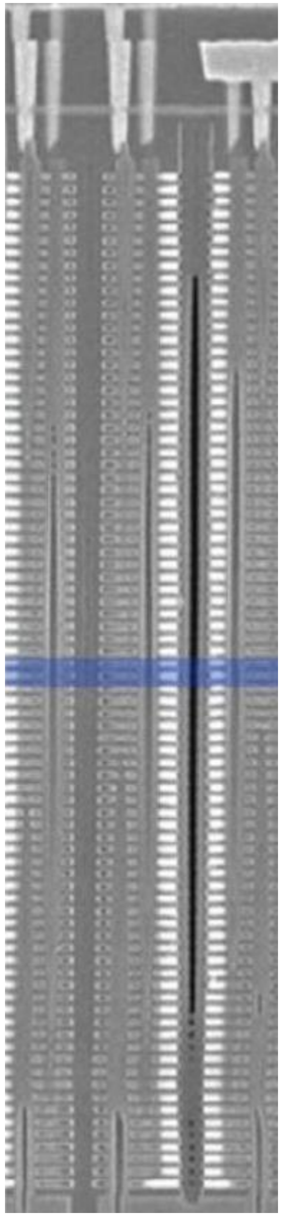
Further Applications for HAR-ALD:

➔ 3D NAND Flash memory is the leading non-volatile memory

➔ Memory cells are stacked: bit density grows by adding layers/tiers

➔ Phase-change memory (PCM) density will improve with 3D architectures enabled by ALD*

*Cheng *et al.*, *JVSTA* **37** (2019) 020907
*Adinolfi *et al.*, *ACS Nano* **13** (2019) 10440



James and Choe, "TechInsights memory technology update", *IEDM 2018*

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